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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,976	12/03/2001	Hamid Reza Rategh	M-12366 US	7816

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EXAMINER
GARBOWSKI, LEIGH M

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/004,976	RATEGH ET AL.	
	Examiner	Art Unit	
	Leigh Marie Garbowski	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 03 December 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Objections

Claims 4-8 are objected to because of the following informalities: as per claims 4-7, --of-- should be inserted after "circuit" [line 1]. As per claim 6, "1" [line 1] should be changed to --3--. As per claim 7, "is" [line 2] should be deleted. As per claim 8, --,-- should be inserted after "system" [line 11]. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Gamal et al. [U.S. Patent #5,754,826].

As per claim 1, Gamal et al. disclose a method comprising: generating a schematic for the IC, comprising a set of transistors [column 6, lines 39-47]; entering data representing each transistor of the set into a CAD system [column 6, lines 39-47]; identifying a first subset of the set of transistors wherein the transistors of the first subset are expected to be subject to voltage levels beyond the bounds of a power rail and a ground rail of the IC during normal operation [column 8, lines 33-46, 53]; designating robust geometries for the transistors of the first subset [column 8, lines 33-46]; and operating the CAD system to generate at least one mask [column 12, lines 20-24]. As per claim 2, Gamal et al. further disclose identifying a second subset of the set of transistors, wherein the second subset are input-output transistors [column 8, lines

33-46]; and designating robust geometries for the transistors of the second subset [column 8, lines 33-46].

As per claim 3, Gamal et al. disclose an IC comprising: a semiconductor die formed using at least one mask designed by the acts of: generating a schematic for the IC, comprising a set of transistors [column 6, lines 39-47]; entering data representing each transistor of the set into a CAD system [column 6, lines 39-47]; identifying a first subset of the set of transistors wherein the transistors of the first subset are expected to be subject to voltage levels beyond the bounds of a power rail and a ground rail of the IC during normal operation [column 8, lines 33-46, 53]; designating robust geometries for the transistors of the first subset, such that the set of data may be used to generate a plurality of masks for lithography of features having mutually different minimum line widths [column 8, lines 33-53; column 12, lines 20-24]. As per claim 4, Gamal et al. further disclose identifying a second subset of the set of transistors, wherein the second subset are input-output transistors [column 8, lines 33-46]; and designating robust geometries for the transistors of the second subset [column 8, lines 33-46]. As per claims 5-6, Gamal et al. further disclose wherein the IC implements a radio frequency circuit/hybrid circuit [column 8, lines 52-53]. As per claim 7, Gamal et al. further disclose wherein the semiconductor die comprises metal-oxide transistors formed using lithography [column 12, lines 20-24].

As per claim 8, Gamal et al. disclose a method comprising: generating a schematic for the IC, comprising a set of transistors [column 6, lines 39-47]; entering data representing each transistor of the set into a CAD system [column 6, lines 39-47];

identifying a first subset of the set of transistors wherein the transistors of the first subset are expected to be subject to voltage levels beyond the bounds of a power rail and a ground rail of the IC during normal operation [column 8, lines 33-46, 53]; designating robust geometries for the transistors of the first subset [column 8, lines 33-46]; and operating the CAD system to generate a first mask associated with a first feature size technology and a second mask associated with a second feature size technology, wherein a respective geometry of each transistor of the first subset is the same for both the first mask and the second mask [column 8, lines 33-53; column 12, lines 20-24].

Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Dangelo et al. [U.S. Patent #5,598,344].

As per claim 1, Dangelo et al. disclose a method comprising: generating a schematic for the IC, comprising a set of transistors [column 1, lines 50-57]; entering data representing each transistor of the set into a CAD system [column 1, lines 50-57]; identifying a first subset of the set of transistors wherein the transistors of the first subset are expected to be subject to voltage levels beyond the bounds of a power rail and a ground rail of the IC during normal operation [column 51, lines 58-59; column 53, lines 39-41]; designating robust geometries for the transistors of the first subset [column 51, lines 64-66; column 53, lines 39-41]; and operating the CAD system to generate at least one mask [column 42, line 35]. As per claim 2, Dangelo et al. further disclose identifying a second subset of the set of transistors, wherein the second subset are

input-output transistors [column 51, lines 2-3, 25-30]; and designating robust geometries for the transistors of the second subset [column 51, lines 2-3, 25-30].

As per claim 3, Dangelo et al. disclose an IC comprising: a semiconductor die formed using at least one mask designed by the acts of: generating a schematic for the IC, comprising a set of transistors [column 1, lines 50-57]; entering data representing each transistor of the set into a CAD system [column 1, lines 50-57]; identifying a first subset of the set of transistors wherein the transistors of the first subset are expected to be subject to voltage levels beyond the bounds of a power rail and a ground rail of the IC during normal operation [column 51, lines 58-59; column 53, lines 39-41]; designating robust geometries for the transistors of the first subset, such that the set of data may be used to generate a plurality of masks for lithography of features having mutually different minimum line widths [column 42, line 35; column 51, lines 64-66; column 53, lines 39-44]. As per claim 4, Dangelo et al. further disclose identifying a second subset of the set of transistors, wherein the second subset are input-output transistors [column 51, lines 2-3, 25-30]; and designating robust geometries for the transistors of the second subset [column 51, lines 2-3, 25-30]. As per claims 5-6, Dangelo et al. further disclose wherein the IC implements a radio frequency circuit/hybrid circuit [column 51, lines 58-59]. As per claim 7, Dangelo et al. further disclose wherein the semiconductor die comprises metal-oxide transistors formed using lithography [column 17, lines 20-21; column 42, line 35].

As per claim 8, Dangelo et al. disclose a method comprising: generating a schematic for the IC, comprising a set of transistors [column 1, lines 50-57]; entering

data representing each transistor of the set into a CAD system [column 1, lines 50-57]; identifying a first subset of the set of transistors wherein the transistors of the first subset are expected to be subject to voltage levels beyond the bounds of a power rail and a ground rail of the IC during normal operation [column 51, lines 58-59; column 53, lines 39-41]; designating robust geometries for the transistors of the first subset [column 51, lines 64-66; column 53, lines 39-41]; and operating the CAD system to generate a first mask associated with a first feature size technology and a second mask associated with a second feature size technology, wherein a respective geometry of each transistor of the first subset is the same for both the first mask and the second mask [column 42, line 35; column 53, lines 39-44].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Baghai et al. disclose "Challenges in CMOS Mixed-Signal Designs for Analog Circuit Designers." Berkcan et al. disclose "Physical Assembly for Analog Compilation of High Voltage ICs."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 703-305-9753. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 703-308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.

Leigh M. Garbowski
Primary Examiner
June 23, 2003

LEIGH M. GARBOWSKI
PATENT EXAMINER